APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,105	10/08/2003	Kenji Abe	1448.1044	4450

21171 7590 10/27/2006	EXAMINER	
STAAS & HALSEY LLP	RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _16 August 2006_.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-12_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-12_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _16 August 2006_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _6/7/06_.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claims 1-12 are present for examination.

Priority

The priority date, 10/09/2002 is being used for this examination.

Drawings

The drawings are accepted at this time since there does not seem to be any

further issues with the drawings that would render a further objection requiring

correction or further explanation to overcome.

Information Disclosure Statement

Acknowledgment is made that the applicant provided an Information Disclosure

Statement (IDS) to the office after the first office action and subsequent examination of

the instant application. It is noted that this IDS includes the European Search Report

and the references noted within said Search Report. The first office action to applicant

was mailed on 2/21/2006, the IDS being acknowledged was received 6/7/2006.

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are

moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

Claims 6 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6, it is unclear to the examiner as the claim stands how less then one validation item can be extracted. Examiner recommends replacing "where n is a positive integer lager then one" with, "wherein n or the less validation items extracted is a positive lager then or equal to one integer" to indicate that either n or the less validation items extracted are never less then one.

As per claim 7, it is unclear to the examiner what the converting unit converts the functional block diagram of the target apparatus to since the limitation stops short of explaining/claiming what the functional block diagram of the target apparatus is converted to before going into the graph which includes a plurality of nodes and edges. Appropriate correction or explanation is required for understanding.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kita

et al. (U.S. Patent 5870590) provided to the office within applicant IDS filed on

(6/7/2006) which is acknowledged as being Applicant Admitted Prior Art (AAPA).

1.   As per claims 1, 11, and 12, Kita teaches an apparatus that supports a validation

of a target apparatus including a plurality of functional devices by generating an

input/output sequence for the target apparatus, comprising:

        Inputting functional configuration information that represents a function of

an apparatus to be validated (column 4 lines 34-62 with column 1 lines 17-19,

column 8 line 45 – column 9 line15, and figures 1, 3, and 8);

        Inputting a condition for the input/output sequence (column 4 lines 34-62

with column 1 lines 17-19, column 8 line 45 – column 9 line15, and figures 1, 3,

and 8);

        Generating unit that generates a validation item function based on the

functional configuration information and the condition (column 4 lines 34-62 with

column 1 lines 17-19, column 8 line 45 – column 9 line15, and figures 1, 3, and

8);

        An extracting unit that extracts a combination of functional devices as a

validation item, from the validation item function (column 4 lines 34-62 with

column 1 lines 17-19, column 8 line 45 – column 9 line15, and figures 1, 3, and

8); and

Generating unit that generates the input/output sequence based on the

validation item (column 4 lines 34-62 with column 1 lines 17-19, column 8 line 45

– column 9 line15, and figures 1, 3, and 8).

Kita does not specifically teach wherein the apparatus comprises:

A first unit for inputting the functional configuration information that

represents a function of an apparatus to be validated;

A second input unit for inputting the condition for the input/output

sequence;

A first generating unit that generates the validation item function based on

the functional configuration information and the condition;

A second generating unit that generates the input/output sequence based

on the validation item.

However those of ordinary skill in the art at the time the invention was made

would recognize that having separate first and second input units and generating units

for supplying the functional configuration information, the condition, generating a

validation item function based on the functional configuration information and the

condition, and generating the input/output sequence based on the validation item

respectively is well know. Additionally it would have been obvious to one having

ordinary skill in the art at the time the invention was made to have separate first and

second input units and generating units, since it has been held that mere duplication of

the essential working part of a device involves only routine skill in the art. *St. Regis*

Paper Co. v. Bemis Co. , 193 USPQ 8. Examiner notes that those of ordinary skill in the

art at the time the invention was made would recognize that at least one input unit and generating unit is required within the apparatus taught by Kita.

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated to incorporate within the apparatus taught by Kita separate first and second input units and generating units for supplying the functional configuration information, the condition, generating a validation item function based on the functional configuration information and the condition, and generating the input/output sequence based on the validation item to implement parallel processing which would decrease processing time and overall execution of testing and/or testing pattern/program/sequence generation.

2.   As per claim 2, Kita as modified teaches the apparatus as described above.

Kita as modified does not specifically teach wherein the validation item function is expressed by a binary decision diagram.

However those of ordinary skill in the art at the time the invention was made would recognize that expressing the validation item function by a binary decision diagram is well know. Examiner notes that binary decision diagrams representing functions has been a well know way to illustrate functions within the art, the art is replete with references.

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated to express the validation item function by a binary decision diagram within the Kita as modified apparatus to allow users to easily understand and/or follow the validation item function.

3.   As per claim 3, Kita as modified teaches the apparatus wherein the condition

includes a resource constraint condition for the functional devices (see Kita column 8

line 45 – column 9 line15).

4.   As per claim 4, Kita as modified teaches the apparatus wherein the condition

includes a condition that limits the functional devices to be included in the validation

item (column 4 lines 34-62 with column 1 lines 17-29, column 8 line 45 – column 9

line15, and figures 1, 3, and 8).

5.   As per claims 5 and 6, Kita as modified teaches the apparatus wherein the

extracting unit extracts a plurality of validation items, n or less validation items, where n

is a positive integer larger then one based on a priority of each of the validation items,

the priority being calculated based on a priority assigned to each of the functional

devices (column 4 lines 19-66 with column 1 lines 17-29, column 8 line 45 – column 9

line15, column 11 lines 40-45, and figures 1, 3, and 8).

6.   As per claim 7, Kita as modified teaches the apparatus as described above.

        Kita as modified does not specifically teach the apparatus further comprising:

            A converting unit that converts a functional block diagram of the target

        apparatus a graph including a plurality of nodes and a plurality of edges, wherein

        the graph is input to the apparatus as the functional configuration information.

        However those or ordinary skill in the art at the time the invention was made

would recognize that a graphical input of a plurality of nodes and edges as the

functional configuration information is well know.

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated to incorporate within the Kita as modified apparatus a graphical input of a plurality of nodes and edges as the functional configuration information so that a user can monitor and know at any time section of the input graph the corresponding value of all the configuration information.

7.   As per claim 8, Kita as modified teaches the apparatus as described above.

Kita as modified does not specifically teach the apparatus further comprising:

A third input unit for inputting a validation environment that defines a flow of data that is input to and output from the target apparatus, wherein the second generating unit that generates the input/output sequence, based on the validation environment and the validation item.

However those of ordinary skill in the art at the time the invention was made would recognize that a third input unit for inputting a validation environment that defines a flow of data that is input to and output from the target apparatus, wherein the second generating unit that generates the input/output sequence, based on the validation environment and the validation item is well known. Examiner notes that those of ordinary skill in the art at the time the invention was made would recognize that a validation item must be tested/examined agents a plurality of conditions which produce errors.

Therefore those of ordinary skill in the art at the time the invention was made would have been motivated to incorporate within the Kita as modified apparatus a third input unit for inputting a validation environment that defines a flow of data that is input to

and output from the target apparatus, wherein the second generating unit that

generates the input/output sequence, based on the validation environment and the

validation item so that the item can be fully tested/examined against a plurality of

conditions which may produce/revile errors and/or configured to operate in conjunction

with other circuitry.

8.   As per claims 9 and 10, Kita as modified teaches the apparatus wherein the

apparatus is connected, via a network, to an information terminal from which the

functional configuration information, the condition, and the validation environment are

input and to which the validation item and the input/output sequence are output (see

figure 1 and column 8 lines 19-41).

Conclusion

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

i.   WIPO (00/072145 A1) as provided to the office within the IDA filed

on 6/7/06 discloses designing a finite state machine model of a system

represented by a graph, enabling a designer to model by defining the

states and connecting them together with directional lines, generating

testing programs corresponding to detected paths to identify system

design flaws, defining the model's behavior with incorporated variables

and expressions, Boolean expressions of the required expression(s),

required expression(s), sub-models with a model, and priority (see figure

9).

  ii. Cohen (U.S. Patent 5542043) as provided to the office within the IDA filed on 6/7/06 discloses user defined relationships between elements within a system, binary tables/truth tables, and networking.

  iii. Applicants Admitted Prior Art (AAPA) within the U.S. Publication 2004/0073859 discloses extracting the input/output sequence from a functional block diagram created by using a predetermined description language, the block diagram expresses the functional device and data flow between functional devices, test pattern creation, graph creation by replacing the functional devices and the data flow with nodes and edges respectively.

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 6/7/06 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of
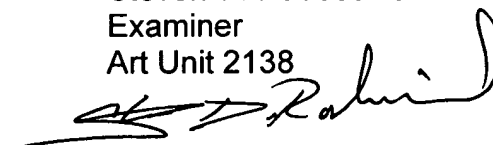
the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
Examiner
Art Unit 2138

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100